

- 1 -

**Title: SEMICONDUCTOR MULTICHIP MODULE PACKAGE WITH
IMPROVED THERMAL PERFORMANCE; REDUCED SIZE AND
IMPROVED MOISTURE RESISTANCE**

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5 RELATED APPLICATIONS

This application is related to and claims priority to Provisional Application
Serial No. 60/190,143 filed March 17, 2000.

FIELD OF THE INVENTION

10 This invention relates to semiconductor devices and more specifically relates
to novel semiconductor device package structures and packaging methods for
multichip modules.

BACKGROUND OF THE INVENTION

15 Multichip semiconductor modules ("MCMs") are known and generally
consist of a plurality of interconnected semiconductor die mounted on a substrate to
form small power conditioning circuits such as d-c to d-c converters, power supplies
for portable electronic equipment and the like.

20 It is very desirable in such devices to minimize electrical resistance due to
packaging (die free package resistance or DFPR); to maximize chip foot print ratios;
to improve the thermal resistance R_{th} of the package; and to improve package
reliability and manufacturability.

BRIEF SUMMARY OF THE INVENTION

In accordance with the invention; a number of novel package innovations, which can be used separately or in combination are provided.

Thus, a "liquid metal" mold cap (a conductive metal-filled epoxy, for example) is provided with vertical insulation barriers separating the top contacts of selected chips while still improving DFPR. The conductive, or liquid metal electrode may be cast with fins to improve cooling.

The chip-foot print ratio is maximized by "tomb-stoning" (or erecting vertically) elongated passive components and by stacking die atop one another.

Thermal resistance is improved by forming fin structures in the top conductive contact, or in an insulation mold cap. Tall passives on the substrate are preferably moved to the center of the substrate and between finned areas.

Reliability and manufacturability is substantially improved by using mold locks to lock the insulation cap onto and telescoping over an organic substrate which receives semiconductor die.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-section of an MCM package with insulated liquid metal top contacts segments for minimized DFPR.

Figure 2 is a cross-section of an MCM package in which passive components are tomb-stoned to minimize chip-foot print ratios.

Figure 3 is a cross-section of an MCM package in which the mold cap is finned to improve the thermal resistance R_{th} .

Figure 4 is a cross-section of an MCM package in which the top cap telescopes over the substrate with a mold lock to improve moisture resistance of the package.

DETAILED DESCRIPTION OF THE DRAWINGS

Referring first to Figure 1, there is shown an MCM package comprised of an organic or other substrate 10 which contains suitable conductive vias (not shown) connecting conductive electrodes such as electrodes 13, 14, 15 on the top of substrate 10 to respective BGA solder balls on the bottom of the substrate, such as BGA solder balls 16, 17 and 18. Two semiconductor die 20 and 21 are mounted on the substrate 10 and may be flip-chip power MOSFET die having their source contacts and gate contacts on the bottom of the die and in contact, through suitable vias, with appropriate ones of the solder balls 16, 17 and 18. The tops of die 20 and 21 are immersed in "liquid metal" (eg. copper or silver powder filled epoxy) top contacts 30 and 31 which are insulated from one another by insulation dams 32, 33, 34. The bottoms of chips 20 and 21 are further insulated by insulation underfill 35 and 36. The top contacts 30 and 31 are connected to the drain electrodes of die 20 and 21 (which are vertical conduction devices) respectively and are connected to suitable contacts on the top of substrate 10 and then to suitable bottom solder balls.

While die 20 and 21 are shown as vertical conduction MOSFETs, they can be any other die, for example, IGBTs; thyristors; diodes and the like, having power electrodes on opposite respective surfaces of the die.

The structure described above for Figure 1 may also use copperstrap conductors of the kind shown in U.S. Patent No. 6,040,626 to decrease top metal resistance and eliminate wire resistance. Further, the novel structure reduces DFPR. The liquid metal contacts may be cast with fins in their top surface if desired.

Figure 2 shows a second embodiment of the invention. In Figure 2, as well as Figures 3 and 4, reference numerals describing similar elements have similar identifying numerals. Figure 2 first shows an insulation mold cap 40 which encloses the top of substrate 10 and all components mounted on the surface. Thus, in Figure 2, two semiconductor die 41 and 42 are shown stacked atop one another and soldered

or conductively cemented to a conductive trace 15 on substrate 10 and wire bonded to appropriate via terminals on substrate 10. Devices 41 and 42 may be diverse devices, for example, a MOSFET and a diode (or an integrated circuit chip if desired). Two passive components, a capacitor C4 and resistor 50 are also fixed to
5 via terminals 53 and 54 respectively on substrate 10. Note that resistor 50 can be erected in tomb-stone fashion (with its longest dimension perpendicular to the mounting surface) as shown by dotted line 51 to reduce the area (or "foot print") needed for the substrate 10.

Figure 3 shows a further embodiment of the invention in which the thermal
10 resistance R_{th} of the package is improved by forming fins 60 and 61 in the insulation cap 40. Note that tall passives, such as capacitor C4 are placed centrally between fin valleys and that the substrate surface above C4 does not contain fins (which would excessively increase the height of insulation cap 40). Note further that die 41 and 42 of Figure 2 are spread apart in Figure 3.

Figure 4 shows a further embodiment of the invention in which the insulation
15 mold cap 40 has a flange 60 which telescopes over the substrate 10. Suitable notches 70, 71 can be formed in the vertical surface of substrate 10. This novel structure produces a mold lock for top cap 40 to insulation substrate 10 and increases the length of the moisture path from the exterior of the package to the sealed components
20 therein. Thus, the novel structure improves package reliability and manufactureability.

Although the present invention has been described in relation to particular
embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present
25 invention be limited not by the specific disclosure herein, but only by the appended claims.